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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,690	01/16/2004	Richard L. Black	P/10-658	8450

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EXAMINER	
ROMAN, LUIS ENRIQUE	
ART UNIT	**PAPER NUMBER**
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,690	BLACK, RICHARD L.	
	Examiner	Art Unit	
	Luis Roman	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's amendment filed on 08/16/07 has been entered. Accordingly claims 3-8, 11-14 have been kept original, claims 9-10 have been amended and claims 1-2 have been previously presented. Claims 15-19 have been added new. It also included remarks/arguments.

The objections to claims 1-2 & 9-10 have been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 & 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (US 6285235) in view of Coats, Jr. (US 3970869).

Regarding claim 1 Ichikawa discloses a gate control circuit for power switching transistor (Fig. 23) wherein the power switching transistor (1) has a control electrode (G) and two main electrodes (C & E), the circuit comprising: a sensing circuit (20, 21, 22, 18a, 18b, 13, 4, 4A, 3E) including a protection switch (3E) for sensing the rate of change of voltage (dv/dt) with respect to time at one of the main electrodes of the power switching transistor (20) and for controlling a protection switch (3E) a sensor that senses the rate of change (dv/dt) (20) which is compared to a threshold (21, 22).

Ichikawa discloses the circuit having an overcurrent protection but is silent or is not clearly explained how it performs it.

Coats, Jr. teaches an overcurrent protecting circuit for a transistor that removes a control signal to the control electrode of the power switching transistor to turn off the power switching transistor if overcurrent is present (Col. 3 lines 50-62 & Fig. 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ichikawa device with the overcurrent protection circuit of Coats, Jr. because it prevents damages on the power transistor.

Regarding claim 2 Ichikawa discloses the circuit of claim 1.
Ichikawa further teaches the sensing circuit comprises a capacitor coupled to a main electrode of the power switching transistor and a resistor coupled to receive a pulse of current from said capacitor (inherently disclosed<see above>), such that a voltage sensed turns on the protection switch wherein the protection switch is turned on if the voltage sensed exceeds a predefined value (Col. 10 line 60 to Col. 11 line 9). For claim 10 the RC circuit is inherently disclosed (see above).

Regarding claim 3 Ichikawa discloses the circuit of claim 2.
Ichikawa further discloses wherein the protection switch comprises a transistor (Fig. 23 element 3E).

Regarding claim 4 Ichikawa discloses the circuit of claims above and further teaches wherein the protection switch comprises a bipolar junction transistor (Fig. 23 element 3E).

Regarding claim 8 Ichikawa discloses the circuit of claims above and further teaches wherein the power switching transistor comprises a field effect transistor (FET) (Col. 1 lines 12-17).

Claims 9-11 & 14-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (US 6285235) in view of Carver (US 3727148).

Regarding claims 9 & 15 in addition to claim 1 Ichikawa does not specifically disclose the configuration of having an storage capacitor and a sensing capacitor coupled to the power switch, wherein the sensing capacitor generates a current representative of the rate of change of voltage of the storage capacitor, a sensing resistor which receives the current from the sensing capacitor and a protection transistor to turn off the power switch if the rate of change exceeds a threshold.

Carver teaches a circuit for overload protection (Col. 1 lines 23-44, Col. 4 lines 28-45 & Figs. 1 & 2) which has an storage capacitor (C5) and a sensing capacitor (C1) coupled to the power switch (Q12), wherein the sensing capacitor generates a current representative of the rate of change of voltage of the storage capacitor (note that the equation that relates dv/dt and a capacitor C is: $v = 1/C (\int i \times dt) \rightarrow dv/dt = i/C$), a sensing resistor (R6) which receives the current from the sensing capacitor and a protection transistor (Q9) to turn off the power switch if the rate of change exceeds a threshold (Col. 4 lines 28-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ichikawa device with the overcurrent protection circuit of Carver because it transmits the power safely (Col. 1 lines 23-44).

Regarding claims 10-11, 14 & 16-19 Carver further teaches that the sensing resistors develops a voltage to turn on the protection transistor when the voltage exceeds a threshold (Col. 4 lines 28-45), the protection transistor is a bipolar junction transistor (Fig. 2 element Q9), the storage capacitor coupled between a main electrode of the power switch transistor and a common (Fig. 2 element C5), the protection (sensing) capacitor is coupled to a main electrode of the power switch transistor (Fig. 2 element C1), and the protection resistor is coupled to the control electrode of the protection switch (Fig. 2 element R6). Ichikawa further discloses wherein the power switch transistor is a field effect transistor (FET) (Col. 1 lines 12-17).

Claims 5-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (US 6285235) in view of Coats, Jr. (US 3970869) and Heminger et al. (US 5751052).

Regarding claims 5-6 Ichikawa in view of Coats, Jr. discloses the circuit of claims above but does not disclose wherein the resistor is coupled across the base-emitter junction of the protection transistor and a diode coupled across the base-emitter junction of the protection transistor to discharge the capacitor.

Heminger et al. teaches wherein the resistor is coupled across the base-emitter junction of the protection transistor (Fig. 1 elements 11, 14) and a diode coupled across the base-emitter junction of the protection transistor to discharge the capacitor (Fig. 1 elements 11, 13).

It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Ichikawa in view of Coats, Jr. with the teachings of Heminger et al. because this configuration protects the transistors against leakage and spikes (Heminger et al.<Col. 1 line 61 to Col. 2 line 5>).

Claim 7 is rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (US 6285235) in view of Coats, Jr. and Ohura et al. (US 5818281).

Regarding claim 7 Ichikawa in view of Coats, Jr. discloses the circuit of claims above but does not teach wherein the protection switch comprises a field effect transistor JFET.

Ohura et al. teaches a protection circuit wherein the protection switch is a FET (Fig. 5 element 2).

It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Ichikawa Coats, Jr. with the teachings of Ohura et al. because it allows a higher switching speed (Ohura et al. <Col. 1 lines 12-16>).

Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (US 6285235) in view of Carver (US 3727148) and Heminger et al. (US 5751052).

Regarding claims 12 Ichikawa in view of Coats, Jr. discloses the circuit of claims above but does not disclose wherein the resistor is coupled across the base-emitter junction of the protection transistor.

Heminger et al. teaches wherein the resistor is coupled across the base-emitter junction of the protection transistor (Fig. 1 elements 11, 14).

It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Ichikawa in view of Coats, Jr. with the teachings of Heminger et al. because this configuration protects the transistors against leakage and spikes (Heminger et al.<Col. 1 line 61 to Col. 2 line 5>).

Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (US 6285235) in view of Carver (US 3727148) and Ohura et al. (US 5818281).

Regarding claim 13 Ichikawa in view of Carver discloses the circuit of claims above but does not teach wherein the protection switch comprises a field effect transistor JFET.

Ohura et al. teaches a protection circuit wherein the protection switch is a FET (Fig. 5 element 2).

It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Ichikawa Carver with the teachings of Ohura et al. because it allows a higher switching speed (Ohura et al. <Col. 1 lines 12-16>).

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luis E. Román whose telephone number is (571) 272-5527. The examiner can normally be reached on Mon – Fri from 7:15 AM to 3:45 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from Patent Application Information Retrieval (PAIR) system.

Status information for unpublished applications is available through private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

Luis E. Román
Patent Examiner
Art Unit 2836

LR/103007

11/8/07

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